Rad-Hard and ULP FPGA with "Full" Functionality, Phase II



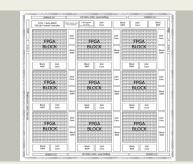
Completed Technology Project (2012 - 2017)

Project Introduction

RNET has demonstrated the feasibility of developing an innovative radiation hardened (RH) and ultra low power (ULP) field programmable gate array (FPGA), called the RH/ULP FPGA. The design utilizes an advanced SOI process technology. It is the vision of RNET to develop a family of radiation hardened FPGA products with a variety of features including programmable logic, configurable analog functions, soft/hardcore microprocessor, dedicated DSP functions, I/O, dedicated memory blocks, memory controllers, global clock, and JTAG interface. In addition, specialized circuits for mitigation of TID/temperature effects, radiation hardened by design SEU techniques, and memory scrubbing are planned. Our vision at the conclusion of this proposed SBIR is to fabricate a "commercial" RH/ULP FPGA with the most important features listed. Ideally the FPGA to be developed under the proposed Phase 2 would contain all of these features, but due to the limitation of funds and allotted time, a scaled down version would be completed. The envisioned device will incorporate the basic programmable logic functions, dedicated block RAM, DSP functions, configurable I/O, global clock distribution network, and JTAG interface. Phase 2 will set the stage for more feature-rich product families to be developed as commercialization continues.

Primary U.S. Work Locations and Key Partners





Rad-Hard and ULP FPGA with "Full" Functionality, Phase II

Table of Contents

Project Introduction	1
Primary U.S. Work Locations	
and Key Partners	1
Images	2
Organizational Responsibility	2
Project Management	2
Technology Maturity (TRL)	3
Technology Areas	3
Target Destinations	3



Small Business Innovation Research/Small Business Tech Transfer

Rad-Hard and ULP FPGA with "Full" Functionality, Phase II

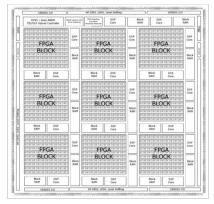


Completed Technology Project (2012 - 2017)

Organizations Performing Work	Role	Туре	Location
RNET Technologies, Inc.	Lead Organization	Industry	Dayton, Ohio
Marshall Space Flight Center(MSFC)	Supporting Organization	NASA Center	Huntsville, Alabama

Primary U.S. Work Locations	
Alabama	Ohio

Images



Briefing Chart Image

Rad-Hard and ULP FPGA with "Full" Functionality, Phase II (https://techport.nasa.gov/imag e/134805)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

RNET Technologies, Inc.

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Principal Investigator:

Todd S Grimes

Co-Investigator:

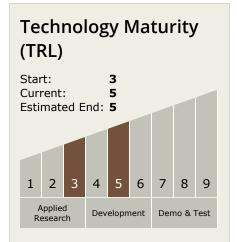
Todd Grimes



Rad-Hard and ULP FPGA with "Full" Functionality, Phase II



Completed Technology Project (2012 - 2017)



Technology Areas

Primary:

- TX10 Autonomous Systems
 - ☐ TX10.3 Collaboration and Interaction
 - └ TX10.3.4 Operational Trust Building

Target Destinations

The Moon, Mars, Outside the Solar System, The Sun, Earth, Others Inside the Solar System

